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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/609,386	07/01/2003	Frank Lin	VIAP0090USA	9347

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EXAMINER	
RUTZ, JARED IAN	
ART UNIT	**PAPER NUMBER**
2187	

DATE MAILED: 01/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/609,386	LIN ET AL.	
	Examiner	Art Unit	
	Jared I. Rutz	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,6,7,9-13,17,18,20-32,35-37 and 40* is/are rejected.

7)☒ Claim(s) *3-5, 8, 14-16, 19, 33-34, and 38-39* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-40 are pending in the instant application. Applicant's arguments filed 11/15/2005 have been carefully and fully considered by the examiner, however they are not persuasive. Accordingly, this action is made **FINAL**.

Priority

2. The supplemental application data sheet submitted on 11/15/2005 is sufficient to correct the error in the priority claim in the declaration filed 7/1/2003. The record is clear that this application claims priority to US provisional application 60/440,046.

Specification

3. The amendment to the specification is sufficient to overcome the examiner's objection to the specification. Accordingly, the objection to the specification has been withdrawn.

Claim Rejections - 35 USC § 102

4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. **Claims 1, 2, 6, 7, 9-13, 17, 18, 20-29, 30-32, 35-37, and 40** are rejected under 35 U.S.C. 102(e) as being anticipated by Van Hook et al (US 6,564,304).

6. **Claim 1** is taught by Van Hook as:

a. A method for accessing a memory device of a computer system, the memory device being electrically connected to a memory controller. Column 3 lines 50-52.

b. The memory controller sequentially responding to a master device according to a sequence of access requests issued in order by the master device. Column 4 lines 32-34.

c. The memory controller comprising a request queue. Column 4 lines 42-44.

d. And a latency monitoring unit electrically connected to the request queue. Column 4 lines 44-47.

e. The method comprising: (a) using the request queue to store access requests generated from the master device. Column 4 lines 42-44.

f. (b) Using the latency monitoring unit to record a plurality of latency values, the latency values respectively corresponding to the access requests stored in the request queue. Column 4 lines 39-41 shows that latency information is stored in the request cue.

g. (c) Using the memory controller to receive a first access request and add the first access request to the request queue with an associated queue priority according to latency values associated with the access requests already stored in the request queue. See column 5 lines 54-55, which shows that the reordering takes the latency into account.

h. And (d) using the memory controller to sequentially access the memory device according to the associated queue priorities of the access requests stored in the request queue. Column 5 lines 64-65 show that the requests are executed in the selected order.

7. **Claim 2** is taught by Van Hook as:

i. The method of claim 1 wherein step (c) further comprises: determining that the first access request is used to access a first page of the memory device. Column 3 lines 54-55 show that the instructions are reordered so that page switches are minimized, therefore it is inherent that the page accessed is determined.

j. And determining if a second access request used to access the first page of the memory device and a third access request used to access a second page of the memory device have been stored in the request queue, the third access request immediately following the second access request and having a queue priority lower than a queue priority of the second access request. The sort queue determines which banks of memory are accessed by each request as part of its sorting algorithm so that page switches are minimized (column 3 lines 54-55).

8. **Claim 6** is taught by Van Hook as:

k. The method of claim 2 wherein step (c) further comprises: if the second access request stored in the request queue corresponds to a lowest queue priority, adding the first access request to the request queue with the lowest queue priority, and assigning an initial value to a first latency value corresponding

to the first access request. Column 5 lines 12-14 show that the latency requirements are taken into account as well as the bank switching. The only way to insert the first access request that takes bank switching and latency into account is after the second access request. Column 4 lines 39-41 show that latency requirements are provided to the request queue, which would be an initial value for the latency.

9. **Claim 7** is taught by Van Hook as:

l. The method of claim 2 wherein step (c) further comprises: if the request queue is empty, adding the first access request to the request queue, and assigning an initial value to a first latency value corresponding to the first access request. Column 4 lines 63-65 states that the requests are provided to the sort queue. Column 4 lines 39-41 show that latency requirements are provided to the request queue, which would be an initial value for the latency.

10. **Claim 9** is taught by Van Hook as:

m. The method of claim 1 wherein the memory device is a main memory of the computer system. Column 3 lines 56-58 state that the memory request controller is provided in a combined CPU and graphics processing architecture.

11. **Claim 10** is taught by Van Hook as:

n. The method of claim 9 wherein the main memory is dynamic random access memory (DRAM). Column 5 lines 21-22.

12. **Claim 11** is taught by Van Hook as:

o. The method of claim 1 wherein the memory controller is positioned within a north bridge circuit of the computer system. Column 3 lines 56-58 state that the memory request controller is provided in a combined CPU and graphics processing architecture. This type of memory controller is referred to as a northbridge in the art. A northbridge definition from Whatis.com is cited as a supporting reference.

13. **Claim 12** is taught by Van Hook as:

p. A method of accessing a memory device of a computer system through a memory controller. Column 3 lines 50-52.

q. The memory controller sequentially responding to a master device according to a sequence of access requests issued in order by the master device. Column 4 lines 32-34.

r. The method comprising: (a) storing access requests generated from the master device in a request queue; Column 4 lines 42-44.

s. (b) recording a plurality of latency values, the latency values respectively corresponding to the access requests stored in the request queue. Column 4 lines 39-41 shows that latency information is stored in the request cue.

t. (c) receiving a first access request and adding the first access request to the request queue with an associated queue priority according to latency values associated with the access requests already stored in the request queue. See column 5 lines 54-55, which shows that the reordering takes the latency into account.

u. And (d) sequentially accessing the memory device according to the associated queue priorities of the access requests stored in the request queue. Column 5 lines 64-65 show that the requests are executed in the selected order.

14. **Claim 13** is taught by Van Hook as:

v. The method of claim 12 wherein step (c) further comprises: determining that the first access request is used to access a first page of the memory device. Column 3 lines 54-55 show that the instructions are reordered so that page switches are minimized, therefore it is inherent that the page accessed is determined.

w. And determining if a second access request used to access the first page of the memory device and a third access request used to access a second page of the memory device have been stored in the request queue, the third access request immediately following the second access request and having a queue priority lower than a queue priority of the second access request. The sort queue determines which banks of memory are accessed by each request as part of its sorting algorithm so that page switches are minimized (column 3 lines 54-55).

15. **Claim 17** is taught by Van Hook as:

x. The method of claim 2 wherein step (c) further comprises: if the second access request stored in the request queue corresponds to a lowest queue priority, adding the first access request to the request queue with the lowest queue priority, and assigning an initial value to a first latency value corresponding to the first access request. Column 5 lines 12-14 show that the latency

requirements are taken into account as well as the bank switching. The only way to insert the first access request that takes bank switching and latency into account is after the second access request. Column 4 lines 39-41 show that latency requirements are provided to the request queue, which would be an initial value for the latency.

16. **Claim 18** is taught by Van Hook as:

y. The method of claim 13 wherein step (c) further comprises: if the request queue is empty, adding the first access request to the request queue, and assigning an initial value to a first latency value corresponding to the first access request. Column 4 lines 63-65 states that the requests are provided to the sort queue. Column 4 lines 39-41 show that latency requirements are provided to the request queue, which would be an initial value for the latency.

17. **Claim 20** is taught by Van Hook as:

z. The method of claim 1 wherein the memory device is a main memory of the computer system. Column 3 lines 56-58 state that the memory request controller is provided in a combined CPU and graphics processing architecture.

18. **Claim 21** is taught by Van Hook as:

aa. The method of claim 9 wherein the main memory is dynamic random access memory (DRAM). Column 5 lines 21-22.

19. **Claim 22** is taught by Van Hook as:

bb. The method of claim 1 wherein the memory controller is positioned within a north bridge circuit of the computer system. Column 3 lines 56-58 state that

the memory request controller is provided in a combined CPU and graphics processing architecture. This type of memory controller is referred to as a northbridge in the art. A northbridge definition from Whatis.com is cited as a supporting reference.

20. **Claim 23** is taught by Van Hook as:

cc. A memory controller for accessing a memory device of a computer system, the memory device being electrically connected to a memory controller, the memory controller sequentially responding to a master device according to a sequence of access requests issued in order by the master device. Column 4 lines 32-34

dd. The memory controller comprising: a request queue for storing access requests generated from the master device. Column 4 lines 42-44.

ee. A latency monitoring unit electrically connected to the request queue for recording a plurality of latency values, the latency values respectively corresponding to the access requests stored in the request queue. Column 4 lines 39-41 shows that latency information is stored in the request cue.

ff. And a reorder decision-making unit electrically connected to the request queue for controlling a first access request added to the request queue with an associated queue priority according to latency values associated with the access requests already stored in the request queue. Column 4 lines 44-47 shows that an arbitrator decides the how to order the memory requests. Column 5 lines 54-55 shows that the latency is taken into account.

gg. Wherein the memory device is sequentially accessed according to the associated queue priorities of the access requests stored in the request queue. Column 5 lines 64-65 show that the requests are executed in the selected order.

21. **Claim 24** is taught by Van Hook as:

hh. The memory controller of claim 23 further comprises: a page/bank comparing unit electrically connected to the reorder decision-making unit and the request queue for determining that the first access request is used to access a first page of the memory device and determining if a second access request used to access the first page of the memory device and a third access request used to access a second page of the memory device have been stored in the request queue, wherein the third access request immediately follows the second access request and has a queue priority lower than a queue priority of the second access request. The sort queue determines which banks of memory are accessed by each request as part of its sorting algorithm so that page switches are minimized (column 3 lines 54-55).

22. **Claim 25** is taught by Van Hook as:

ii. The memory controller of claim 24 further-comprising: a latency control unit electrically connected to the reorder decision-making unit and the latency monitoring unit for detecting whether a third latency value corresponding to the third access request is greater than a maximum allowance value. Column 3 line 66 to column 4 line 3 shows that latency requirements are considered when

requests are reordered. This shows that a reorder will not be made if it prevents a request from meeting its latency requirements.

23. **Claim 26** is taught by Van Hook as:

jj. The memory controller of claim 25 wherein the maximum allowance value is programmable. The latency value is programmed by the master that makes the access request (column 4 lines 39-41).

24. **Claim 27** is taught by Van Hook as:

kk. The method of claim 1 wherein the memory device is a main memory of the computer system. Column 3 lines 56-58 state that the memory request controller is provided in a combined CPU and graphics processing architecture.

25. **Claim 28** is taught by Van Hook as:

ll. The method of claim 9 wherein the main memory is dynamic random access memory (DRAM). Column 5 lines 21-22.

26. **Claim 29** is taught by Van Hook as:

mm. The method of claim 1 wherein the memory controller is positioned within a north bridge circuit of the computer system. Column 3 lines 56-58 state that the memory request controller is provided in a combined CPU and graphics processing architecture. This type of memory controller is referred to as a northbridge in the art. A northbridge definition from Whatis.com is cited as a supporting reference.

27. **Claim 30** is taught by Van Hook as:

nn. A method for accessing a memory device of a computer system, the method comprising: receiving one or more access requests for accessing the memory device in a first predetermined order; and reordering the access requests in a second predetermined order to be processed in a request queue by relocating a first access request to follow a second access request accessing a same memory page. Column 3 lines 54-55 show that requests are reordered to minimize page switches. In order to reorder, there must be a first predetermined order that is reordered to provide a second predetermined order.

oo. Wherein the relocating is prohibited if it increases a processing latency for a third access request to exceed a predetermined limit. Column 3 line 66 to column 4 line 3 shows that latency requirements are considered when requests are reordered. This shows that a reorder will not be made if it prevents a request from meeting its latency requirements.

28. **Claim 31** is taught by Van Hook as:

pp. The method of claim 30 wherein the third access request immediately follows the second access request in the request queue before the first access request is inserted. Using the definitions of second and first access requests as given in claim 2 "the third access request immediately following the second access request and having a queue priority lower than a queue priority of the second access request" this is inherent in the stated claim.

29. **Claim 32** is taught by Van Hook as:

qq. The method of claim 30 wherein the reordering further includes: identifying that the first and the second access requests access the same memory page; determining that the third access request is for accessing a different memory page. The sort queue determines which banks of memory are accessed by each request as part of its sorting algorithm so that page switches are minimized (column 3 lines 54-55).

rr. And inserting the first access request between the second and the third access requests in the request queue. Column 3 lines 54-55 state that instructions are reordered so that page switches are reordered. Column 5 lines 12-14 show that the latency requirements are taken into account as well as the bank switching. The only way to insert the first access request that takes bank switching and latency into account is between the second and third access requests.

30. **Claim 35** is taught by Van Hook as:

ss. The method of claim 30 wherein the maximum latency value is programmable. The latency value is programmed by the master that makes the access request (column 4 lines 39-41).

31. **Claim 36** is taught by Van Hook as:

tt. A method for accessing a memory device of a computer system, the method comprising: receiving one or more access requests for accessing the memory device, the access requests accessing one or more memory pages; and arranging the access requests in a predetermined order to be processed in a

request queue by putting one or more access requests together for accessing a same memory page consecutively in one or more groups. Column 3 lines 54-55.

uu. Wherein an access request is prohibited from being grouped to be processed before at least one other access request if the grouping increases a processing latency of the at least one other access request in the request queue to exceed a predetermined limit. The memory controller takes into account the latency requirements of the memory requests (column 3 line 66 to column 4 line 3.)

32. **Claim 37** is taught by Van Hook as:

vv. The method of claim 36 wherein the arranging further includes: identifying that a first access request received after a second access request accesses the same memory page as the second access request; determining that a third access request is for accessing a different memory page; inserting the first access request between the second and the third access requests in the request queue; and repeating the above identifying, determining and inserting steps for all received access requests. Column 3 lines 54-55 state that instructions are reordered so that page switches are reordered. Column 5 lines 12-14 show that the latency requirements are taken into account as well as the bank switching. The only way to insert the first access request that takes bank switching and latency into account is between the second and third access requests.

33. **Claim 40** is taught by Van Hook as:

ww. The method of claim 36 wherein the maximum latency value is programmable. The latency value is programmed by the master that makes the access request (column 4 lines 39-41).

Allowable Subject Matter

34. **Claims 3-5, 8, 14-16, 19, 33-34, and 38-39** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

35. **Claims 3 and 14** recite the limitation "increasing the third latency value by a predetermined increment value". Although the invention disclosed by Van Hook considers the latency requirements of a memory access request, it does not disclose changing the latency value associated with a request to reflect the change in the latency due to a reorder.

36. **Claims 4-5 and 15-16** depend on the instant claims and are allowable for the reasons discussed supra with respect to claims 3 and 14.

37. With respect to **claims 8 and 19**, the record is clear as to the reasons for allowability.

38. **Claims 33 and 38** recite the "limitations examining whether the latency value associated with the third access request is increased to exceed the predetermined limit if the first access request is to be inserted" and "increasing the latency value associated with the third access request by a predetermined incremental value if the first access request is inserted." These steps are not taught by Van Hook.

Claims 34 and 39 depend on the instant claims and are allowable for the reasons discussed supra with respect to claims 33 and 38.

Response to Arguments

39. Applicant's arguments filed 11/15/205 have been fully considered but they are not persuasive.

First Point of Argument

40. In lines 5-15 of page 5, Applicant argues that Van Hook teaches that each memory master has it's own request queue and the request queue is coupled to the memory controller, and that Van Hook does not teach that the memory controller comprises a request queue as claimed. The examiner respectfully disagrees. The combination of the memory controller, request queue, and sort queue as taught by Van Hook are equivalent to the memory controller as claimed.

Second Point of Argument

41. In lines 17-22 of page 5, Applicant argues that Van Hook teaches that the latency information is provided in the request queue, and as such Van Hook does not teach that a latency monitoring unit is electrically connected to the request queue. The examiner respectfully disagrees. Column 4 lines 39-47 show that latency information is stored in the request queue, and an arbitrator decides how to order the memory requests from the request queues. The portion of the request queue holding the latency information and the arbitrator form the latency monitoring unit as claimed.

Third Point of Argument

42. In lines 24 of page 5 through line 3 of page 6, Applicant argues that Van Hook teaches that the latency information is provided in the request queue, and therefore does not teach that the latency values are recorded in the latency monitoring unit which is electrically connected to the request queue. The examiner respectfully disagrees. The portion of the request queue holding the latency information and the arbitrator as taught by van Hook are equivalent to the latency monitoring unit as claimed.

Fourth Point of Argument

43. In lines 5-15 of page 6, Applicant argues that Van Hook does not teach that the latency values of the access request already stored in the request queue are taken into consideration when ordering a new request. The examiner respectfully disagrees. Column 5 lines 9-13 of Van Hook show that the latency requirements of the masters (provided in the request queue) are taken into account when reordering the memory requests.

Fifth Point of Argument

44. In lines 17-24 of page 6, Applicant argues that Van Hook teaches that if a higher priority request occurs, the request accessed is terminated, and that this differs from the instant application. The examiner respectfully disagrees. There is no suggestion in the cited section of Van Hook that the request accessed is terminated. Additionally, this argument is not commiserate with the language of the claim, as claim 1 does not require or prohibit terminating access requests.

Sixth Point of Argument

45. In lines 26 of page 6 through line 5 of page 7, Applicant argues that Van Hook does not teach that requests with the same page are put together. The examiner respectfully disagrees. Column 3 lines 54-55 and column 8 lines 11-13 show that requests for memory access are reordered to minimize page breaks. In order to minimize page breaks, reads and writes to the same page are grouped together.

Seventh Point of Argument

46. In lines 7-18 of page 7, Applicant argues that Van Hook does not teach that the latency values of the access request already stored in the request queue are taken into consideration when ordering a new added request. The examiner respectfully disagrees. Column 6 lines 32-36 of Van Hook state "The servicing of a request queue continues until a higher priority queue exists or the selected queue is invalid." By selecting to service a higher priority queue, the arbitrator is adding a new request to the sort queue with an associated queue priority according to latency values associated with the access requests already stored in the request queue. The higher priority requests are added to the sort queue before a lower priority request.

Eighth Point of Argument

47. In lines 19-25 of page 7, Applicant argues that Van Hook teaches that if a higher priority request occurs, the request accessed is terminated. The examiner respectfully disagrees. There is no suggestion in the cited section of Van Hook that the request accessed is terminated. Additionally, this argument is not commiserate with the language of the claim, as claim 2 does not require or prohibit terminating access requests.

Ninth Point of Argument

48. In lines 1-6 of page 8, Applicant argues that Van Hook does not teach that requests with the same page are put together. The examiner respectfully disagrees. Column 3 lines 54-55 and column 8 lines 11-13 show that requests for memory access are reordered to minimize page breaks. In order to minimize page breaks, reads and writes to the same page are grouped together.

Tenth Point of Argument

49. In lines 8-16 of page 8, Applicant argues that Van Hook teaches that the latency information is provided in the request queue, and therefore does not teach that the latency values are recorded in the latency monitoring unit which is electrically connected to the request queue. The examiner respectfully disagrees. The portion of the request queue holding the latency information and the arbitrator as taught by van Hook are equivalent to the latency monitoring unit as claimed.

Eleventh Point of Argument

50. In lines 18-25 of page 8, Applicant argues that Van Hook teaches that if a higher priority request occurs, the request accessed is terminated. The examiner respectfully disagrees. There is no suggestion in the cited section of Van Hook that the request accessed is terminated. Additionally, this argument is not commiserate with the language of the claim, as claim 23 does not require or prohibit terminating access requests.

Twelfth Point of Argument

51. In lines 1-7 of page 9, Applicant argues that Van Hook does not teach that a page/bank comparing unit is electrically connected to the reorder decision-making unit. The examiner respectfully disagrees. Column 5 lines 44-53 shows that the memory controller reorders memory requests taking into account page and bank accesses. Additionally, the examiner directs Applicant to the sixth point of argument supra, which discusses grouping accesses by page.

Thirteenth Point of Argument

52. In lines 9-21, Applicant argues that with respect to claim 25 Van Hook does not teach that a reorder will not be made if a new added request will make the latency value of an already stored request in the request queue exceed a maximum allowance value. The examiner respectfully disagrees. Column 5 lines 54-59 of Van Hook show that a higher priority request will stop a write burst. A write burst is a series of consecutive writes to a page or bank of memory. If there is a higher priority request than the write to be performed, the higher priority request takes precedence. This shows the memory controller detecting whether the latency value corresponding to the third request (the request accessing a different page than the first and second requests) is greater than the allowable latency.

Conclusion

53. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jared I. Rutz whose telephone number is (571) 272-5535. The examiner can normally be reached on M-F 8:00 AM - 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jared I Rutz
Examiner
Art Unit 2187

jir

DONALD SPARKS
SUPERVISORY PATENT EXAMINER